REMARKS

Claims 1-20 are currently pending in this application. Claim 1-3 and 5-20 have been rejected on various grounds as discussed below. Claim 4 has been objected to, and the Examiner has indicated that it would be allowable if rewritten in independent form including all limitations of its base claim and any intervening claims.

By the present response, Claims 1, 5, 6, 9, 13, and 17 have been amended. Reconsideration of Claims 1-20 as amended is respectfully requested in view of the following remarks.

Claim 5 was rejected under 35 U.S.C. 112 on the basis that the limitation "the HBUSREQ signal" lacked antecedent basis. By the present amendment Claim 5 has been amended to refer to "an HBUSREQ signal". With this amendment, Claim 5 meets the requirements of 35 U.S.C. 112.

Claim 6 was rejected under 35 U.S.C. 112 on the basis that the limitation "the HBUSGRANT signal" lacked antecedent basis. By the present amendment Claim 6 has been amended to refer to "an HBUSGRANT signal". With this amendment, Claim 6 meets the requirements of 35 U.S.C. 112.

Claims 1 and 17 were rejected under 35 U.S.C. 102(e) as being anticipated by Lo et al. U.S. Patent 6,425,071 Lo('071), the Examiner alleging that Lo('071) discloses an ASIC having an internal bus operating at a first clock frequency and a bridge coupling signals from the internal bus to an off-chip device operating at a second clock frequency. The Applicant respectfully traverses these rejections as they would apply to the amended Claims 1 and 17.

Claims 1 and 17 have been amended to clearly distinguish the disclosure of Lo('071). Each claim now includes a processor on the integrated circuit. Each claim now limits the

internal bus to an Advanced Microcontroller Bus Architecture Advanced High-performance Bus. Each claim is now limited to the chip internal bus operating at a frequency higher than the off chip device.

The Lo('071) reference teaches a system in which a RISC processor operating with an ARM ASB bus is on one chip and a separate ASIC, i.e. a second chip, is used solely for converting signals from ARM ASB bus protocol to PCI protocol. The PCI protocol operates at a frequency higher than the ARM ASB bus protocol. The ARM ASB bus of the Lo('071) reference operates at a low frequency which allows the ARM ASB bus to be connected directly from the RISC processor chip to off chip devices such as the interface circuit 224 disclosed by Lo('071). If the processor 200 of Lo('071) were upgraded to operate with the Advanced Microcontroller Bus Architecture Advanced High-performance Bus, it would need a bridge on the same chip as the processor 200 to allow the bus signals to be coupled off the chip as taught by the present invention.

The present invention is directed to a problem encountered in integrated circuits operating with the Advanced Microcontroller Bus Architecture Advanced High-performance Bus. The frequency of this bus is higher than the ARM ASB bus protocol and higher than most external devices. Integrated circuits operating with the Advanced Microcontroller Bus Architecture Advanced High-performance Bus normally operate at lower voltages to reduce power dissipation which increases with frequency. The processor and the Advanced Microcontroller Bus Architecture Advanced High-performance Bus must be on the same chip to communicate directly at the high speed and low voltage. The combination of high frequency and low voltage makes it difficult to couple the Advanced Microcontroller Bus Architecture Advanced High-performance Bus signals off the integrated circuit to external devices. Since the

interface of the present invention must couple signals to and from the Advanced Microcontroller Bus Architecture Advanced High-performance Bus, it should be on the same chip as the bus and therefore on the same chip as the processor. The present invention provides a solution to this problem by putting interface circuitry on the same chip as the processor, so that the chip has outputs from the bridge capable of coupling signals to lower speed off chip devices.

In view of these differences from the cited reference, the Applicant submits that Claims 1 and 17 are allowable. Since Claims 2-3 and 5-8 further limit Claim 1 and Claims 18-20 further limit Claim 17, the Applicant submits that Claims 2-3 and 5-8 and Claims 18-20 are also allowable.

Claim 4 was indicated to be allowable if rewritten in independent form. Since Claim 4 depends from Claim 1, which has been shown to be patentable above, the Applicant submits that Claim 4 is also allowable without rewriting in independent form.

Claims 2, 3, 7, 9-16, and 18-20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lo('071), Lo et al. U.S. Patent 6,366,973, (Lo('973)), and AMBA specification version 2.0, in view of Hofmann et al. U.S. Patent 6,633,994 (Hofmann). The applicant respectfully traverses these rejections as they apply to the amended claims.

Regarding Claim 9, the Examiner alleges that Lo('973) discloses a method for coupling signals from an internal bus to an off-chip device comprising loading data into registers and then transferring the data to the off chip device. Further, the Examiner alleges that the AMBA specification discloses detecting the start of a bus write cycle, comparing the address signal to addresses assigned to slave devices, and holding the HREADY signal low until data transfer is complete. The Examiner then alleges that it would be obvious to use the AMBA specification to handle write operations since this would insure the proper operation of the bus.

The Lo('973) reference does not disclose a process for coupling signals from a high speed processor operating with the Advanced Microcontroller Bus Architecture Advanced High-performance Bus to an off chip device. It could not include such a disclosure, since it discloses and claims only an interface circuit which is on a chip separate from the chip with the processor. As noted above, the speed and voltage characteristics of the Advanced Microcontroller Bus Architecture Advanced High-performance Bus make it difficult to directly couple processor signals from the chip to an off chip device. The present invention places a bridge on the same chip as the processor to that the signals can be converted to slower off chip speeds and higher voltages.

In view of these differences, the Applicant submits that Claim 9 is patentable over the cited references. Since Claims 10-12 further limit Claim 9, the Applicant submits that Claims 10-12 are also patentable over the cited references.

Regarding Claim 13, the Examiner alleges that the Lo('973) reference discloses a method for coupling signals from an internal bus to an off chip device comprising loading data into registers and then transferring the data to the internal bus. Further, the Examiner alleges that the AMBA specification discloses a method for detecting the start of a bus read cycle, comparing the address signal to addresses assigned to slave devices, and holding the HREADY signal low until data transfer is complete. The Examiner then alleges that it would be obvious to use the AMBA specification to handle read operations since this would insure the proper operation of the bus.

The Lo('973) reference does not disclose a process for coupling signals from an off chip device to a high speed processor operating with the Advanced Microcontroller Bus Architecture Advanced High-performance Bus. It could not include such a disclosure, since it discloses and claims only an interface circuit which is on a chip separate from the chip with the

processor. As noted above, the speed and voltage characteristics of the Advanced Microcontroller Bus Architecture Advanced High-performance Bus make it difficult to directly couple processor signals from an off chip device to the processor on the chip. The present invention places a bridge on the same chip as the processor to that the signals can be converted from slower off chip speeds and higher voltages to the speeds and voltages needed for the Advanced Microcontroller Bus Architecture Advanced High-performance Bus.

In view of these differences, the Applicant submits that Claim 13 is patentable over the cited references. Since Claims 14-16 further limit Claim 13, the Applicant submits that Claims 14-16 are also patentable over the cited references.

In summary, the Applicant submits that Claims 1-20, as amended, have been shown to be patentable over the cited references.

It is submitted that, upon entry of the present amendment, this application will be in condition for allowance. However, if the Examiner has any questions or comments or otherwise feels it would be helpful in expediting the application, he is encouraged to telephone the undersigned at (972) 731-2288.

The Commissioner is hereby authorized to charge payment of any further fees associated with any of the foregoing papers submitted herewith, or to credit any overpayment thereof, to Deposit Account No. 12-2252, LSI Logic Corporation.

Respectfully submitted,
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